CLAIMS

What is claimed is:

1. A method comprising:

using processor implementation-specific instructions to save a processor state in a system memory when a machine check error is generated by a processor;

attempting to correct the error using processor implementation-specific instructions;

transferring control to processor-independent instructions;

receiving control from processor-independent instructions; and

returning to an interrupted context of the processor by restoring the processor state.

2. The method of claim 1, further comprising providing processor error record information obtained using processor implementation-specific instructions.

3. The method of claim 1, further comprising attempting to contain the error if a second processor is coupled to the processor by requesting a rendezvous between the processor and the second processor.

4. The method of claim 1, wherein receiving control from processor-independent instructions indicates that the error has been corrected.

5. The method of claim 1, further comprising obtaining an address of a location to save the processor state in the system memory provided by platform-specific instructions.

6. The method of claim 1, wherein attempting to correct the error using processor implementation-specific instructions is not done if an expected machine check indicator is set.

7. A machine-readable medium that provides instructions that, if executed by a processor, will cause the processor to perform operations comprising:

using processor implementation-specific instructions to save the processor state in a system memory when a machine check error is generated by the processor;

attempting to correct the error using processor implementation-specific instructions;

transferring control to processor-independent instructions;

receiving control from processor-independent instructions; and

returning to an interrupted context of the processor by restoring the processor state.

8. The machine-readable medium of claim 7, wherein the operations further comprise using processor implementation-specific instructions to provide processor error record information requested by processor-independent instructions.

9. The machine-readable medium of claim 7, wherein the operations further comprise attempting to contain the error if a second processor is coupled to the processor by requesting a rendezvous between the processor and the second processor.

10. The machine-readable medium of claim 7, wherein receiving control from processor-independent instructions indicates that the error has been corrected.

11. The machine-readable medium of claim 7, wherein the operations further comprise obtaining an address of a location to save the processor state in the system memory provided by platform-specific instructions.

12. The machine-readable medium of claim 7, wherein attempting to correct the error using processor implementation-specific instructions is not done if an expected machine check indicator is set.

13. The machine-readable medium of claim 7, wherein the instructions provided by the machine-readable medium are not cacheable by the processor.

14. A central processing unit (CPU) comprising:

a processor;

a first machine-readable medium coupled to the processor, the first machine-readable medium including processor implementation-specific instructions that, if executed by the processor, will cause the processor to perform operations including

saving the processor state in a system memory and attempting to correct the error when a machine check error is generated by the processor, and

receiving control and returning to the interrupted context of the processor by restoring the state of the processor when the error is determined to have been corrected;

a second machine-readable medium coupled to the processor, the second machine-readable medium including only processor implementation-independent instructions that, if executed by the processor, will cause the processor to perform operations including

receiving control from the first machine-readable medium;

determining if the error has been corrected;

transferring control to the first machine-readable medium if the error has been corrected.

15. The central processing unit (CPU) of claim 14, wherein the operations performed by the instructions provided by the second

machine-readable medium further include requesting processor error record information from the first machine-readable medium.

16. The central processing unit (CPU) of claim 14, wherein the operations performed by the instructions provided by the first machine-readable medium further include attempting to contain the error if a second processor is coupled to the processor by requesting a rendezvous between the processor and the second processor.

17. The central processing unit (CPU) of claim 14, wherein the operations performed by the instructions provided by the second machine-readable medium further include providing an address of a location to save the processor state in the system memory to the first machine-readable medium.

18. The central processing unit (CPU) of claim 14, wherein attempting to correct the error is not done if an expected machine check indicator is set.

19. The central processing unit (CPU) of claim 14, wherein the instructions provided by the first and second machine-readable media are not cacheable by the processor.

20. The central processing unit (CPU) of claim 14, wherein the operations performed by the instructions provided by the second machine-readable medium further include if the error is

uncorrected, passing control to an operating system error handler if present, otherwise, performing one of a halt and a reboot of the CPU.